REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed January 8, 2003. Claims 3, 14, 20, and 21 have been cancelled without prejudice, waiver, or disclaimer. Claims 1, 4, 5, 7 - 9, 12, 13, 15, and 19 have been amended. Claim 22 has been added. The subject matter of amended claims 1, 4, 5, 7 – 9, 12, 13, 15, and 19 is contained within Figs. 4 – 13 and the related detailed description of the specification. Consequently, no new matter has been added. Upon entry of the amendments in this response, Claims 1, 2, 4 – 13, 15 – 19, and 22 remain pending. Claims 1, 2, 4 – 13, and 15 – 19 are patentable over the cited art of record. New Claim 22 is patentable over the art of record for at least the reason that the cited art fails to disclose, teach, or suggest a second carry save adder as claimed. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections Under 35 U.S.C. 102

The Office Action indicates that claims 1 – 4, 6 – 10, 12 – 16 and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent 5,389,835 to Yetter, hereafter *Yetter*. Applicant respectfully traverses the rejection of claims 1, 2, 4, 6 – 10, 12, 13, 15, 16 and 18. Applicant has canceled claims 3 and 14. Consequently, the rejection of claims 3 and 14 is rendered moot.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior-art reference disclose each element, feature, or step of the claim. See *e.g.*, *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988).

Concerning claims 1 – 4, 6 – 10, 12 – 16 and 18 the Office Action asserts that *Yetter*, "discloses an apparatus in Figs. 8A and 8B performing the addition of a PKG recoded number (table D in col. 11) . . ." Applicant respectfully submits that claim 1, as amended, is patentable over *Yetter*.

Claim 1

Applicant's claim 1, as amended, recites the following:

> 1. An apparatus performing the addition of a PKG recoded number, said apparatus comprising:
> a circuitry configured to receive at least a first value and a second value; and
> ***a first adder configured to add said first value and said second value, wherein said second value is at least one of a P value, a K value, and a G value of a PKG recoded number*** and said first adder generates a carry-out value and at least one of a P value, a K value and G value of a PKG recoded number wherein said circuitry generates a sum value and a carry value.

(Applicant's independent claim 1 - *Emphasis Added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the features of pending claim 1 highlighted above. Consequently, claim 1 is allowable.

Concerning independent Claim 1, *Yetter* does not disclose teach or suggest, "***a first adder configured to add said first value and said second value, wherein said second value is at least one of a P value, a K value, and a G value of a PKG recoded number.***" FIGs. 8A and 8B of *Yetter* apparently disclose a ternary ripple carry adder that uses intermediary vectors I1 and I2 in a process of converting three input vectors into two output vectors in a vector logic implementation of a ternary ripple carry adder. The three input vectors comprise two non-boolean variables (*i.e.*, A = <A2, A1, A0> and B = <B2, B1, B0>) and a single boolean variable, CI. The two output vectors comprise a single non-boolean variable, S = <S2, S1, S0>, and a single boolean variable, CO. Intermediate vector variables I1 and I2 are used to generate the output vectors. Table I includes a truth table for the mousetrap (*i.e.*, self-timed) logic gate illustrated in the various circuits of FIG. 8B. Table I reveals P, K, and G values used to create intermediate vector variable I1. Variables P, K, and G are a function of the two non-boolean variables A and B and are generated in accordance with three of the circuits illustrated in FIG. 8B as defined in the truth table. As clearly shown above, in the circuits of FIG. 8B, and as described in column 17, lines 51 – 60 of *Yetter,* the P, K, and G values are not added. Consequently, Applicant respectfully

submits that Yetter does not disclose, teach, or suggest Applicant's claimed "***a first adder configured to add said first value and said second value, wherein said second value is at least one of a P value, a K value, and a G value of a PKG recoded number.***" Accordingly, the Office Action rejection of claim 1 should be withdrawn.

Claims 2, 4, and 6

Because independent claim 1 is allowable, its respective dependent claims 2, 4, and 6 are also allowable, as a matter of law, since these dependent claims contain all elements, features, or steps of independent claim 1. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Accordingly, Applicant submits that the rejection of claims 2, 4, and 6 should be withdrawn.

Claim 7

Applicant's claim 7, as amended, recites the following:

> 7. A method for performing the addition of PKG recoded numbers, comprising:
> receiving a first value;
> receiving a second value, wherein said second value is at least one of a P value, a K value, and a G value of a first PKG recoded number; and
> ***generating a sum value including at least one of a P value, a K value and G value of a second PKG recoded number*** and a first carry-out value from said first value and said second value.

(Applicant's independent claim 7 - *Emphasis Added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the features of pending claim 7 highlighted above. Consequently, claim 7 is allowable.

Regarding independent Claim 7, *Yetter* does not disclose teach or suggest, "***generating a sum value including at least one of a P value, a K value and G value of a second PKG recoded number.***" FIGs. 8A and 8B of *Yetter* apparently disclose a ternary ripple carry adder that uses intermediary vectors I1 and I2 in a process of converting three input vectors into two output vectors in a vector logic

implementation of a ternary ripple carry adder. The three input vectors comprise two non-boolean variables (*i.e.*, A = <A2, A1, A0> and B = <B2, B1, B0>) and a single boolean variable, CI. The two output vectors comprise a single non-boolean variable, S = <S2, S1, S0>, and a single boolean variable, CO. Intermediate vector variables I1 and I2 are used to generate the output vectors. Table I includes a truth table for the mousetrap (*i.e.*, self-timed) logic gate illustrated in the various circuits of FIG. 8B. Table I reveals P, K, and G values used to create intermediate vector variable I1. Variables P, K, and G are a function of the two non-boolean variables A and B and are generated in accordance with three of the circuits illustrated in FIG. 8B as defined in the truth table. As clearly shown above, in the circuits of FIG. 8B, and as described in column 17, lines 51 – 60 of *Yetter,* the P, K, and G values are not added. Therefore, *Yetter* does not show generating a sum value using a second PKG recoded number. Consequently, Applicant respectfully submits that *Yetter* does not disclose, teach, or suggest Applicant's claimed "***generating a sum value including at least one of a P value, a K value and G value of a second PKG recoded number.***" Accordingly, the Office Action rejection of claim 7 should be withdrawn.

Claims 8 – 10 and 12

Because independent claim 7 is allowable, its respective dependent claims 8 – 10 and 12 are also allowable, as a matter of law, since these dependent claims contain all elements, features, or steps of independent claim 7. *In re Fine, supra.* Accordingly, Applicant submits that the rejection of claims 8 – 10 and 12 should be withdrawn.

Claim 13

Applicant's claim 13, as amended, recites the following:

> 13. An apparatus for apparatus performing the addition of PKG recoded number, said apparatus comprising:
> means for receiving a first value;
> means for receiving a second value, said second value including at least one of a P value, a K value and G value of a PKG recoded number; and

> ***means for generating a first sum value including at least one of a P value, a K value and G value of a second PKG recoded number and a first carry-out value from said first value and said second value.***

(Applicant's independent claim 13 - *Emphasis Added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the features of pending claim 13 highlighted above. Consequently, claim 13 is allowable.

Concerning independent Claim 13, *Yetter* does not disclose teach or suggest, "***means for generating a first sum value including at least one of a P value, a K value and G value of a second PKG recoded number and a first carry-out value from said first value and said second value.***" FIGs. 8A and 8B of *Yetter* apparently disclose a ternary ripple carry adder that uses intermediary vectors I1 and I2 in a process of converting three input vectors into two output vectors in a vector logic implementation of a ternary ripple carry adder. The three input vectors comprise two non-boolean variables (*i.e.*, A = <A2, A1, A0> and B = <B2, B1, B0>) and a single boolean variable, CI. The two output vectors comprise a single non-boolean variable, S = <S2, S1, S0>, and a single boolean variable, CO. Intermediate vector variables I1 and I2 are used to generate the output vectors. Table I includes a truth table for the mousetrap (*i.e.*, self-timed) logic gate illustrated in the various circuits of FIG. 8B. Table I reveals P, K, and G values used to create intermediate vector variable I1. Variables P, K, and G are a function of the two non-boolean variables A and B and are generated in accordance with three of the circuits illustrated in FIG. 8B as defined in the truth table. As clearly shown above, in the circuits of FIG. 8B, and as described in column 17, lines 51 – 60 of *Yetter,* the P, K, and G values are not added. Therefore, *Yetter* does not show means for generating a first sum including a second PKG recoded number. Consequently, Applicant respectfully submits that Yetter does not disclose, teach, or suggest Applicant's claimed "***means for generating a first sum value including at least one of a P value, a K value and G value of a second PKG recoded number and a first carry-out value from said first value and said second value.***" Accordingly, the Office Action rejection of claim 13 should be withdrawn.

Claims 15, 16, and 18

Because independent claim 13 is allowable, its respective dependent claims 15, 16, and 18 are also allowable, as a matter of law, since these dependent claims contain all elements, features, or steps of independent claim 13. *In re Fine*, *supra*. Accordingly, Applicant submits that the rejection of claims 15, 16, and 18 should be withdrawn.

Rejections Under 35 U.S.C. 103

The Office Action indicates that claims 5, 11, and 17 stand rejected under 35 U.S.C. 103(a) as being obvious over *Yetter*, as applied above, in view of U.S. patent 6,055,557 to Beck, hereafter *Beck*. Applicant respectfully asserts that *Yetter* does not teach, disclose or otherwise suggest each of the elements, limitations, or method steps of the amended independent claims 1, 7, and 13. *Beck* apparently discloses an adder that generates encoded outputs to conserve power. In particular, the adder provides "B2" encoded outputs which only drive one bit per every two bits at a time in a data processing system (*See* Abstract.) As apparently shown in FIG. 3, *Beck* is configured to concatenate two B2 encoded values.

Applicant respectfully asserts that the proposed combination of *Yetter's* ternary ripple carry adder cannot be combined to reach Applicant's claimed apparatus and method for at least the reason that *Yetter* is not configured to receive and add PKG values. Assuming *arguendo* that the circuits of *Yetter* and *Beck* could be combined, for at least the reason that *Beck* fails to remedy the failure of *Yetter* to disclose, teach, or suggest each element, limitation or method step of Applicant's independent claims, claims 5, 11, and 17 which depend therefrom are patentable.

Claim 19

Applicant's claim 19, as amended, recites the following:

> 19. An apparatus performing the addition of PKG recoded numbers, said apparatus comprising:
> a circuitry configured to receive at least one of a P value, a K value and a G value of a first PKG recoded

number and at least one of a P value, a K value and a G value of a second PKG recoded number; and

a first carry save adder configured to generate a first carry-out value and a first result comprising at least one of a P value, a K value and a G value.

(Applicant's independent claim 19 - *Emphasis Added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the features of pending claim 19 highlighted above. Consequently, claim 19 is allowable. Applicant has canceled claims 20 and 21. Consequently, the rejection of claims 20 and 21 is rendered moot.

Concerning independent Claim 19, *Beck* does not disclose teach or suggest, "***a first carry save adder configured to generate a first carry-out value and a first result comprising at least one of a P value, a K value and a G value.***" FIG. 3 of *Beck* apparently discloses a circuit that generates two "B2" encoded results from P, K, and G inputs. The circuit then concatenates the first of the two "B2" encoded results with the second "B2" encoded result. Beck's encoders 304 and 800 illustrated in FIG. 3 are not configured to generate a carry-out value. Therefore, *Beck* does not show a first carry save adder. Consequently, Applicant respectfully submits that *Beck* does not disclose, teach, or suggest Applicant's claimed "***first carry save adder configured to generate a first carry-out value and a first result comprising at least one of a P value, a K value and a G value.***" Accordingly, even if *Yetter* discloses a PKG value from a PKG recode number, the proposed combination still fails to disclose, teach, or suggest Applicant's claim 19. Therefore, the Office Action rejection of claim 19 should be withdrawn.

In addition to the failure of the proposed combination to suggest all features of the claimed invention and forming a second and independent reason for patentability, the Office Action rejection fails to establish a *prima facie* case of obviousness. The initial burden is upon the Patent Office to establish a *prima facie* case of obviousness. Such a *prima facie* showing includes an identification of a proper suggestion or motivation within the prior art to make the combination.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103(a), there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious.

W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ... Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) *In re Dow Chemical Company*, 837 F.2d 469, 473 (Fed. Cir. 1988).

The Federal Circuit has repeatedly stated, "Modification unwarranted by the disclosure of a reference is improper." *Carl Schenck, A.G, v. Nortron Corp.*, 713 F.2d 782, 218 U.S.P.Q. 698, 702 (Fed. Cir. 1983). In this regard, "[t]he mere fact that the prior art may be modified in the manner suggested by the [Office action] does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 U.S.P.Q.2d 1780 (Fed Cir. 1992).

Every invention contains a recitation of elements. Many inventions can be categorized as a new combination of well-known elements. When new combinations are analyzed on an element-by-element basis, each of the elements may already be known. If merely proving that each element of a pending claim were well-known was enough to render the claim obvious, nothing would be patentable.

In the present rejection, the Office Action simply concludes, with no reasoned analysis that one skilled in the art would be motivated to combine the "B2" encoder of *Beck* to the vector logic ternary adder of *Yetter* to "perform more than two operands." Applicant can find no evidence of a suggestion or motivation to combine the vector logic ternary adder of *Yetter* with the "B2" encoder of *Beck*. Similarly, Applicant can find no suggestion or motivation to combine the "B2" encoder of *Beck* with the vector logic ternary adder of *Yetter*. Because, a *prima facie* case of obviousness is established only when there is proper motivation to substitute, modify, or add the

particular missing element from a first reference with the element as found in the second reference, Applicant submits that the Office Action has failed to establish a proper a *prima facie* case of obviousness.

Consequently, Applicant respectfully requests that the Office identify the specific teachings within the prior art that would suggest the desirability or motivation for the particular combination of elements as claimed or withdraw the rejection of claims 5, 11, 17, and 19.

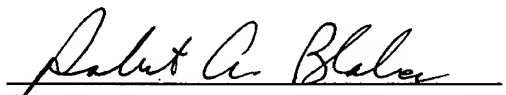
Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1, 2, 4 – 13, 15 – 19, and 22 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,



Robert A. Blaha, Reg. No. 43,502

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
(770) 933-9500

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that is enclosed within brackets ("[ ]") being deleted:

1. (Twice Amended) An apparatus performing the addition of a PKG recoded number, said apparatus comprising:

a circuitry configured to receive at least a first value and a second value [, wherein said second value is at least one of a P value, a K value, and a G value of a PKG recoded number]; and

a first adder configured to add said first value and said second value, wherein said second value is at least one of a P value, a K value, and a G value of a first PKG recoded number and said first adder generates a carry-out value and at least one of a P value, a K value and a G value of a second PKG recoded number and wherein said circuitry generates a sum value and a carry value.

4. (Once Amended) The apparatus of claim 1 [3], wherein said [first value is at least one of a P value, a K value and a G value of a PKG recoded number] circuitry further comprises:

a second adder configured to add said second PKG recoded number from said first adder and a carry-in value.

5. (Twice Amended) The apparatus of claim 1 [3], wherein said first value is at least one of a P value, a K value and a G value of a PKG recoded number.

7. (Twice Amended) A method for performing the addition of PKG recoded numbers, comprising the steps of:

receiving a first value;

receiving a second value, wherein said second value is at least one of a P value, a K value and a G value of a first PKG recoded number; and

generating a sum value including at least one of a P value, a K value and a G value of a second PKG recoded number and a first carry-out value from said first value and said second value.

8. (Twice Amended) The method of claim 7, further comprising [the steps of]:

[adding said first value and said second value;]

forwarding [generating] a first result including at least one of a P value, a K value and a G value from said generating [adding; and

generating a first carry-out value from said adding].

9. (Twice Amended) The method of claim 8, further comprising [the steps of]:

adding said first result and a carry-in value;

generating a final sum value from said adding; and

generating a final carry-out value from said adding.

12. (Twice Amended) The method of claim 7, further comprising [the step of]:

converting at least one dual rail encoded value into said second value.

13. (Twice Amended) An apparatus for apparatus performing the addition of PKG recoded number, said apparatus comprising:

means for receiving a first value;

means for receiving a second value, said second value including at least one of a P value, a K value and G value of a PKG recoded number; and

means for generating a first sum value including at least one of a P value, a K value and a G value of a second PKG recoded number and a first carry-out value from said first value and said second value.

15. (Twice Amended) The apparatus of claim 13 [14], further comprising:

means for adding said first sum value [result] and a carry-in value to generate a final sum value and a final carry-out value.

19. (Twice Amended) An apparatus performing the addition of PKG recoded numbers, said apparatus comprising:

a circuitry configured to receive at least one of a P value, a K value and a G value of a first PKG recoded number and at least one of a P value, a K value and a G value of a second PKG recoded number; and

a first carry save adder configured to generate [wherein said circuitry generates] a first carry-out value and a first result comprising at least one of a P value, a K value and a G value.